QUALIFICATION REQUIREMENTS REMOVED

MIL-M-38510/220A(USAF)
15 November 1983
SUPERSEDING
MIL-M-38510/220(USAF)
26 March 1979

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL,
8192 BIT, MOS, ULTRAVIOLET ERASABLE
PROGRAMMABLE READ-ONLY MEMORY (EPROM)
MONOLITHIC SILICON

This specification is approved for use by Rome Air Development Center, Department of the Air Force, and is available for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic, silicon, N-channel MOS erasable programmable read-only memory microcircuits which employ the ultraviolet light erasing technique. One product assurance class and a choice of case outlines and lead finishes are provided and are reflected in the complete part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510 except the "JAN" or "J" certification shall not be used.

1.2.1 Device type. The device type shall be as follows:

Device type	Circuit
01	1024 X 8 Bit EPROM

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

Outline letter	Case outline (see MIL-M-38510, appendix C)
J	D-3 (24-lead, 1/2" X 1-1/4" dual-in-line package) 1/

1.3 Absolute maximum ratings.

Supply voltage, V_{CC} 2/	-0.3 to 15 V
Supply voltage, V_{DD} 2/	-0.3 to 20 V
Supply voltage, V_{SS} 2/	-0.3 to 15 V
All input voltages (except program and CS (PE)) 2/	-0.3 to 15 V
Program input, 2/	-0.3 to 35 V
CS (PE) input voltage 2/	-0.3 to 20 V

1/ Lid shall be transparent to permit ultraviolet light erasure.

2/ Under absolute maximum ratings, voltage values are with respect to the most negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffis AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

Output voltage (operating, with respect to V_{SS})	-2 to 7 V
Operating free-air temperature range	-55°C to +100°C 3/
Storage temperature range	-65°C to +125°C
Lead temperature (soldering 10 seconds)	300°C
Thermal resistance, junction-to-case	θ_{JC} = 30°C/W
Maximum power dissipation, P_D 4/	1.8 watts dc
Maximum junction temperature	T_J = 160°C

1.4 Recommended operating conditions.

Supply voltage, V_{CC}	+4.5 to +5.5 V dc
Supply voltage, V_{DD}	+10.8 to +13.2 V dc
Supply voltage, V_{BB}	-4.5 to -5.5 V dc
Supply voltage, V_{SS}	GND
Minimum high-level input voltage, V_{IH}	2.4 V dc to V_{CC} +1
Maximum low-level input voltage, V_{IL}	V_{SS} to 0.65 V dc
High-level program enable input voltage $V_{IH(PE)}$	11.4 to 12.6 V
High-level program input voltage, $V_{IH(PR)}$	25 to 27 V
Low-level program input voltage, $V_{IL(PR)}$ ($V_{IL(PR)}$ max ≤ $V_{IH(PR)}$ - 25)	V_{SS} to 1 V
Case operating temperature range	-55°C to +100°C

2. APPLICABLE DOCUMENTS

2.1 Government specifications and standards. Unless otherwise specified, the following specifications and standards, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of specifications, standards, handbooks, drawings, and publications required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting officer.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this specification shall take precedence.

3. REQUIREMENTS

3.1 Detail specifications. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510, and herein.

3.2.1 Terminal connections. Terminal connections shall be as specified on figure 1.

3/ For application when sustained temperature excursions greater than 100°C will occur, periodic reprogramming is recommended.
4/ Must withstand the added P_D due to short circuit test (e.g. I_{OS}).

3.2.2 Truth table.

3.2.2.1 Unprogrammed or erased devices. The truth table for unprogrammed devices shall be as specified on figure 2.

3.2.2.2 Programmed devices. The requirements for supplying programmed devices are not part of this specification.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.2.4 Schematic circuits. The schematic circuits shall be submitted to the qualifying activity as a prerequisite for qualification. All manufacturer's schematics shall be maintained and available upon request.

3.2.5 Case outlines. Case outlines shall be in accordance with MIL-M-38510 and 1.2.3 herein.

3.3 Lead material and finish. Lead material and finish shall be in accordance with MIL-M-38510 (see 6.5).

3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

3.5 Electrical test requirements. Electrical test requirements shall be as specified in table III. The subgroups of table III which constitute the minimum electrical test requirements for screening and quality conformance, by device class, are specified in table II.

3.6 Marking. Marking shall be in accordance with MIL-M-38510. At the option of the manufacturer, marking of the country of origin may be omitted from the body of the microcircuit, but shall be retained on the initial container. The "JAN" or "J" certification mark shall not be used.

3.7 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.7.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.8.

3.7.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.7 and table IV.

3.7.3 Verification of erasure or programmability of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 27 (see MIL-M-38510 appendix E).

3.9 Manufacturer eligibility. To be eligible to supply microcircuits to this specification a manufacturer shall have a manufacturer certification in accordance with MIL-M-38510 for at least one line, not necessarily the line producing the device type described herein.

3.10 Certification. Certification in accordance with MIL-M-38510 is not required for this device.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007 of MIL-STD-883, except as modified herein.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions Unless otherwise specified, T_C = -55°C to +100°C	Limits		Unit
			Min	Max	
High level output voltage	V_{OH1}	V_{CC} = 4.5 V, V_{BB} = -4.5 V, V_{DD} = 10.8 V, V_{IN} = 2.4 V, I_{OH} = -100 µA, V_{SS} = GND	3.7		Volts
High level output voltage	V_{OH2}	V_{CC} = 4.5 V, V_{BB} = -4.5 V, V_{DD} = 10.8 V, V_{IN} = 2.4 V, I_{OH} = -1.0 mA, V_{SS} = GND	2.4		Volts
Low level output voltage	V_{OL}	V_{CC} = 5.5 V, V_{BB} = -5.5 V, V_{DD} = 13.2 V, V_{IN} = 0.65 V, I_{OL} = 1.6 mA, V_{SS} = GND		0.45	Volts
Output leakage current	I_{LO} 2/	V_{CC} = 5.5 V, V_{BB} = -5.5 V, V_{DD} = 13.2 V, V_{OUT} = 5.5 V, $\overline{CS}$(PE) = 2.4 V, P = GND, V_{SS} = GND		10	µA
High level input current	I_{IH}	Address and program enable ($\overline{CS}$(PE)), V_{CC} = 5.5 V, V_{BB} = -5.5 V, V_{DD} = 13.2 V, V_{IN} = 5.5 V, V_{SS} = GND, P = GND		10	µA
Low level input current	I_{IL}	Address and program enable ($\overline{CS}$(PE)), V_{CC} = 5.5 V, V_{BB} = -5.5 V, V_{DD} = 13.2 V, V_{IN} = 0.65 V, V_{SS} = GND, P = GND		10	µA
Output short circuit current	I_{OS} 3/	V_{CC} = 5.5 V, V_{BB} = -5.5 V, V_{DD} = 13.2 V, $\overline{CS}$(PE) = 0.65 V, V_{IN} = 2.4 V, V_{OUT} = GND, V_{SS} = GND		-30	mA
Supply currents	I_{DD}	V_{CC} = 5.5 V, V_{BB} = -5.5 V,		80	mA
	I_{CC}	V_{DD} = 13.2 V, V_{IN} = 2.4 V,		15	mA
	I_{BB}	$\overline{CS}$(PE) = GND, Outputs = open, V_{SS} = GND		60	mA
Propagation delay times $\overline{CS}$(PE) to unprogrammed outputs	t_{PZH}	V_{CC} = 5.5 V, V_{BB} = -5.5 V, V_{DD} = 13.2 V, V_{SS} = GND, C_L = 100 pF, Address and $\overline{CS}$(PE): t_{THL} = t_{TLH} = 20 ns	20	160	ns
	t_{PHZ}	See figure 4. ($\overline{CS}$(PE) = GND for t_{PLH} and t_{PHL} only)	20	160	ns
$\overline{CS}$(PE) to programmed outputs	t_{PZL}		20	160	ns
	t_{PLZ}		20	160	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics 1/ - Continued.

Test	Symbol	Conditions Unless otherwise specified, T_C = -55°C to +100°C	Limits Min	Limits Max	Unit
Propagation delay times Address inputs to outputs (access time)	t_{PLH}	V_{CC} = 5.5 V, V_{BB} = -5.5 V, V_{DD} = 13.2 V, V_{SS} = GND, C_L = 100 pF Address and $\overline{CS}$(PE): t_{THL} = t_{TLH} -20 ns See figure 4. ($\overline{CS}$(PE) = GND for t_{PLH} and t_{PHL} only)	75	450	ns
	t_{PHL}		75	450	ns
Read cycle time	$t_{c(rd)}$		450		ns
Output invalid from address change	t_{PVX}		0		ns
$\overline{CS}$(PE) to unprogrammed outputs	t_{PZH}	V_{CC} = 4.5 V, V_{BB} = -4.5 V, V_{DD} = 10.8 V, V_{SS} = GND, C_L = 100 pF, $t_{f(cs)}$ = $t_{f(ad)}$ = 20 ns, See figure 4. ($\overline{CS}$(PE) = GND for t_{PLH} and t_{PHL} only)	20	160	ns
	t_{PHZ}		20	160	ns
$\overline{CS}$(PE) to programmed outputs	t_{PZL}		20	160	ns
	t_{PLZ}		20	160	ns
Address inputs to outputs (access time)	t_{PLH}		75	450	ns
	t_{PHL}		75	450	ns
Read cycle time	$t_{c(rd)}$		450		ns
Output invalid address change	t_{PVX}		0		ns

1/ DC and read mode.

2/ Connect all address inputs and the $\overline{CS}$(PE) input to V_{IH} and measure I_{LO} with the output under test connected through a current meter to the voltage specified.

3/ Condition the address inputs to set the output under test indicated "H" per the checkerboard truth table to its high voltage state and measure I_{OS} with the output under test connected to a ground through a current meter.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following conditional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883). Test condition D or E using the circuits shown on figure 5, or equivalent.

b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. Percent defective allowable (PDA). The PDA for class B devices shall be 10 percent based on failures from group A, subgroups 1 and 7, test after cooldown as final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre-burn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. The verified failures of group A, subgroups 1 and 7, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent defective for that lot, and the lot shall be accepted or rejected based on the PDA for the applicable device class.

d. A programmability test shall be performed when programming the devices using an LTPD of 10.

e. A bit retention test shall be performed prior to burn-in and shall consist of the following:

1. Program all devices with the complement of the binary count pattern (see 3.7.2 and 4.3d).
2. Verify pattern (see 3.7.3).
3. Remove all device terminal connections (including supply voltages).
4. Perform a high temperature storage for 48 hours at 150°C.
5. Restore device terminal connections.
6. Verify pattern (see 3.7.3).
7. Erase the pattern and program, devices with a binary count pattern (see 3.7.2).
8. Verify pattern (see 3.7.3).
9. Burn-in (see 4.3a).
10. Verify pattern (see 3.7.3) at 25°C, and at 125°C.

f. After completion of all testing, the devices shall be erased and verified prior to delivery (except devices submitted for groups A, B, C, and D testing).

4.3 Qualification inspection. Qualification inspection is not required.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4). Generic test data may be used to satisfy the requirements for group C and D inspections (see 6.7).

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III)
	Class B devices
Interim electrical parameters (pre burn-in) (method 5004)	1
Final electrical test parameters (method 5004)	1*,2,3,7*,9
Group A test requirements (method 5005)	1,2,3,7,8, 9,10,11
Group C end point electrical parameters (method 5005)	1,2,3,7,8
Additional electrical subgroups for group C periodic inspection	None
Group D end point electrical parameters (method 5005)	1,2,3,7,8

NOTES:

1. (*) indicates PDA applies to subgroup 1 and 7 (see 4.2c).
2. Any or all subgroups may be combined when using high-speed testers.
3. Subgroup 7 and 8 shall consist of verifying the binary count pattern.
4. For all electrical tests, the device shall be programmed to the pattern specified.

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I method 5005 of MIL-STD-883 and as follows:

a. Tests shall be as specified in table II.

b. Subgroup 4, 5, and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. All devices selected for testing shall be programmed with a binary count pattern. After completion of all testing the devices shall be erased and verified (except devices submitted for group B, C, and D testing).

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883.

a. All devices selected for testing shall be programmed with a binary count pattern. After completion of all testing, the devices shall be erased and verified (except devices submitted for group C and D testing).

b. A special subgroup shall be added using an LTPD of 15 for classes S, B, and C. This subgroup shall consist of a high voltage test of the input protection circuits, V_{ZAP} (see 4.9).

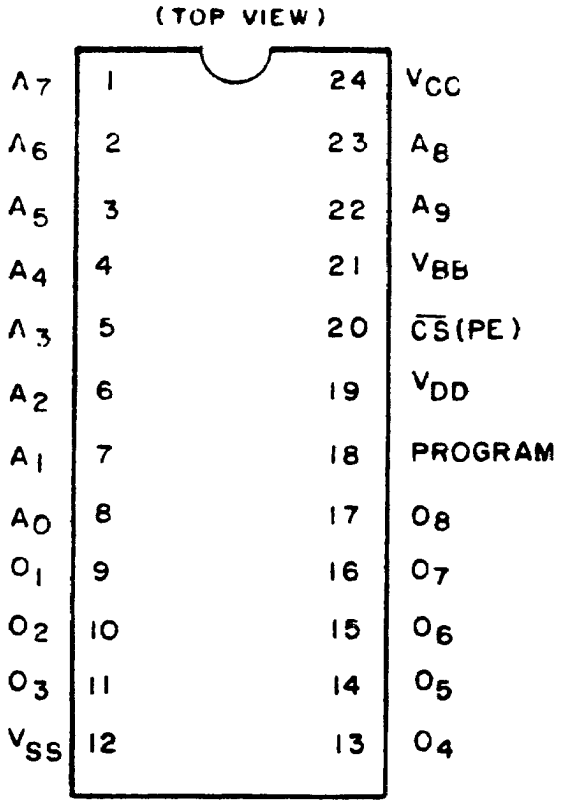


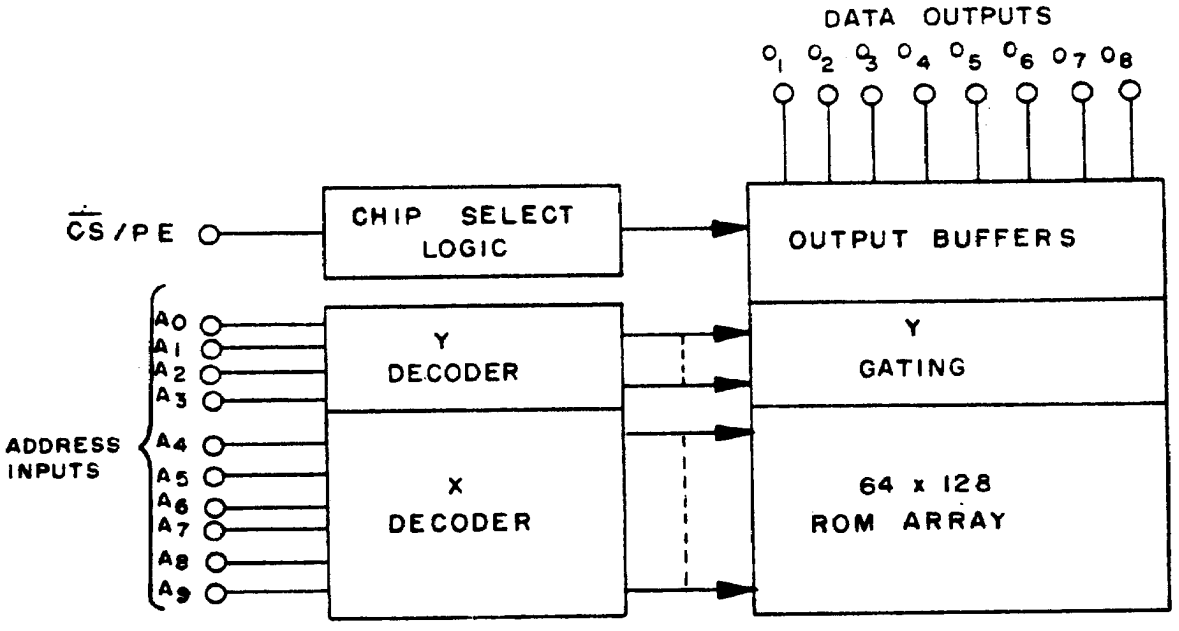
FIGURE 1. Terminal connections.

Truth table (unprogrammed) 1/

Word number	Inputs			Outputs 2/
	Program	$\overline{CS}$(PE)	$A_9A_8A_7A_6A_5A_4A_3A_2A_1A_0$	$Q_8Q_7Q_6Q_5Q_4Q_3Q_2Q_1$
X	V_{SS}	L	← X →	H H H H H H H H
X	V_{SS}	H	← X →	← HI-Z →

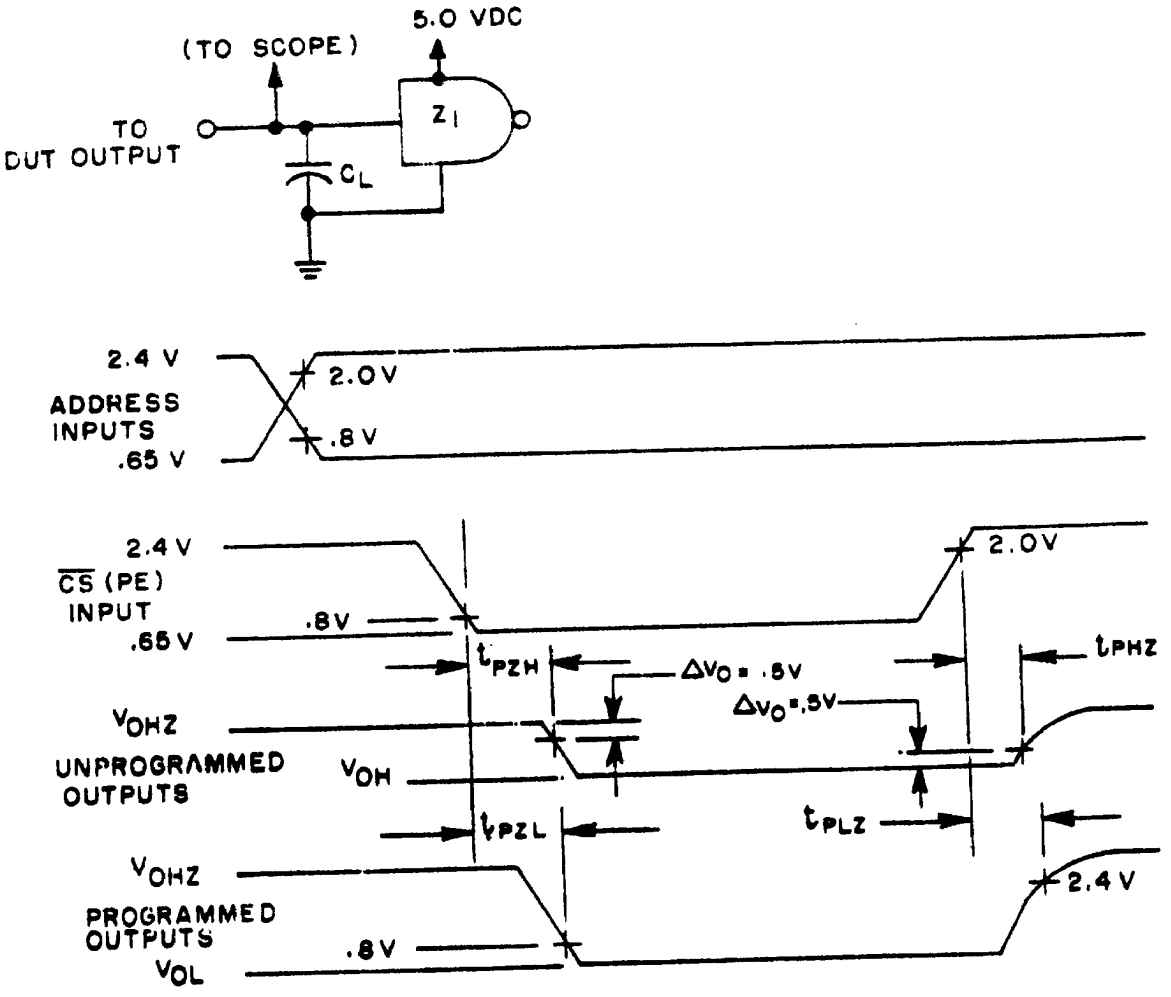
NOTES:
1/ Positive logic: H = high logic level, L = low logic level, X = irrelevant, HI-Z = high-impedance state.
2/ Outputs have internal active pull-ups.

FIGURE 2. Truth table (unprogrammed devices).



NOTES:
1. A_0 = least significant address bit; A_9 = most significant address bit.
2. O_1 = least significant data output bit; O_8 = most significant data output bit.

FIGURE 3. Functional block diagram.



$\overline{CS}$ (PE) INPUTS TO OUTPUTS

NOTES:
1. C_L = 100 pF and includes jig and probe capacitance.
2. Z_1 = 5400 TTL gate or equivalent.

FIGURE 4. Propagation delay time test circuit and waveforms.

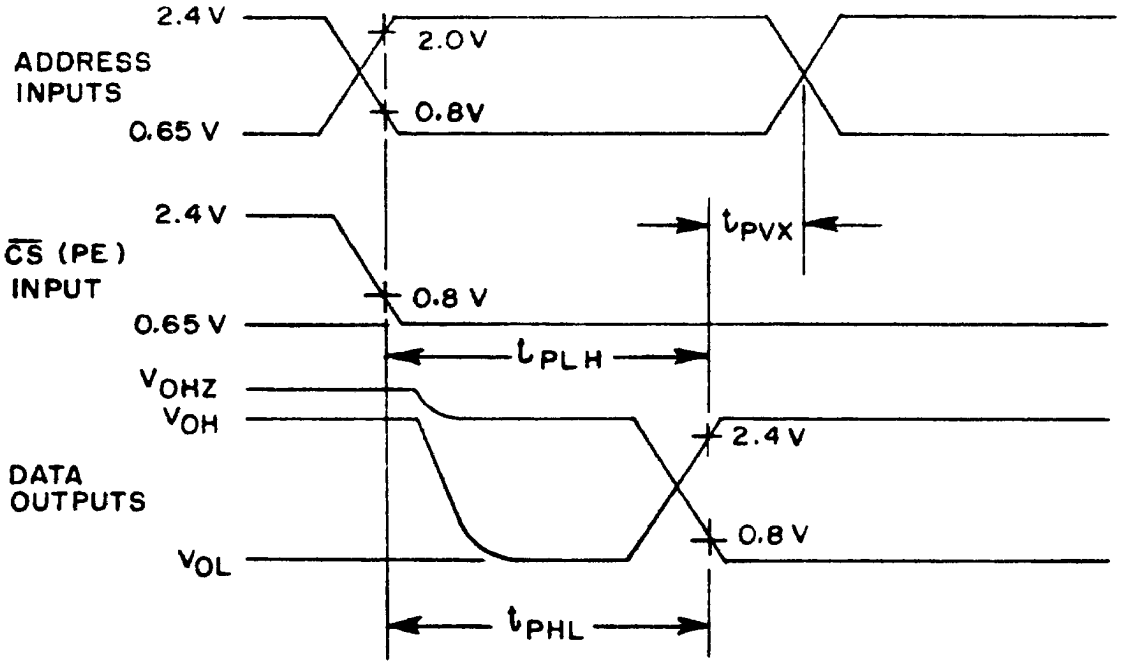
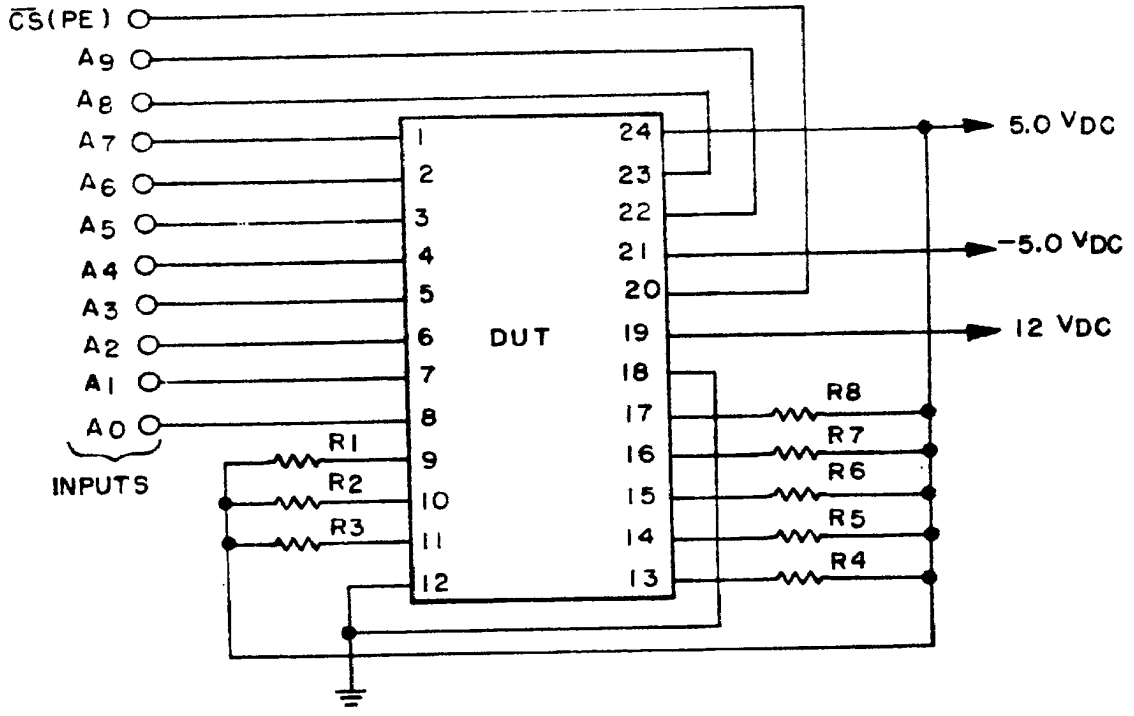


FIGURE 4. Propagation delay time test circuit and waveforms - Continued.

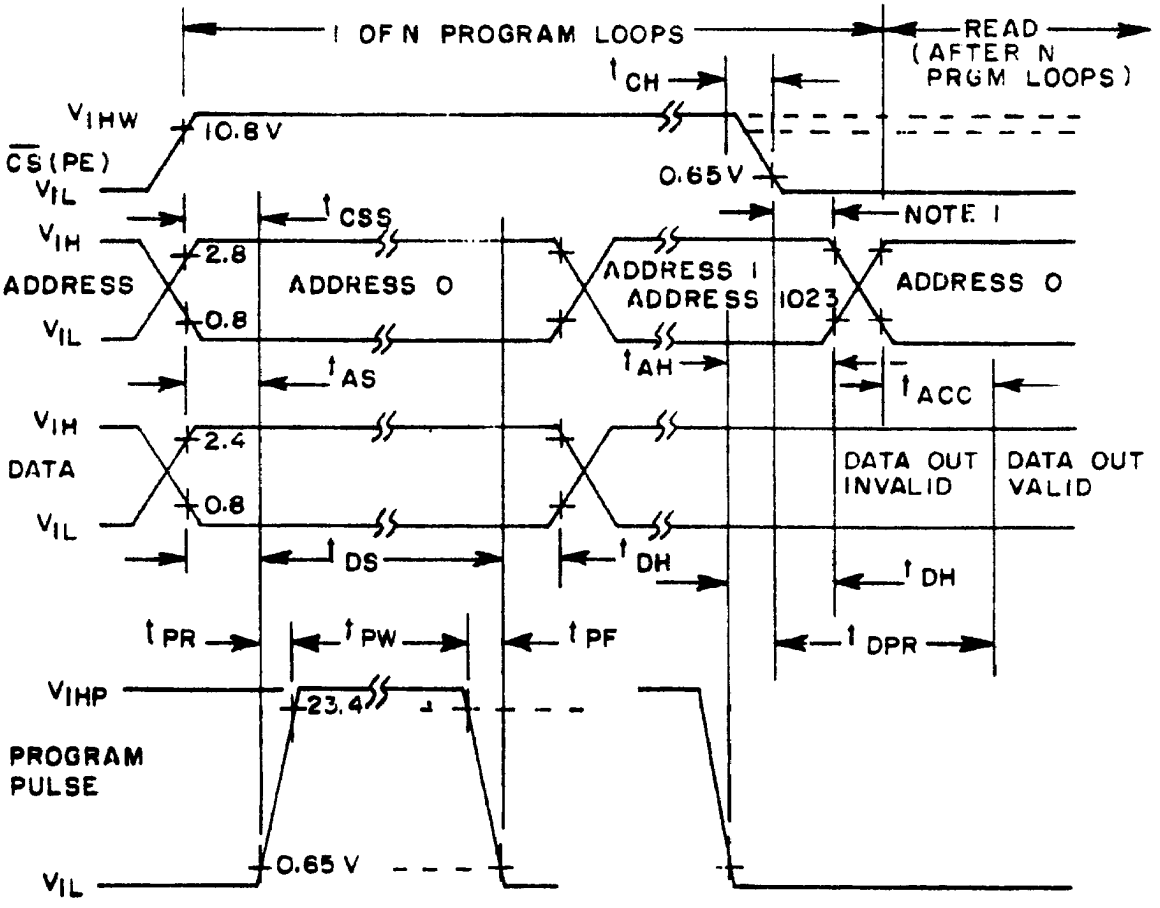


NOTES:
1. R1 thru R8 = 3.6 kΩ ±5.0% when $\overline{CS}$(PE) input is pulsed:
   = 1.0 kΩ ±5.0% when $\overline{CS}$(PE) is at $V_{IH} \geq 2.4$ V
2. Input signal characteristics: amplitude: $V_{IH} \geq 2.4$ V, $V_{IL} \leq 0.4$ V; duty cycle = 50%; $t_{THL} = t_{TLH} \leq 100$ ns and the following PRR (±20%):

Input	PRR	Input	PRR
A_0	16 kHz $\leq f_0 \leq$ 100 kHz	A_7	$f_0 \div 128$
A_1	$f_0 \div 2$	A_8	$f_0 \div 256$
A_2	$f_0 \div 4$	A_9	$f_0 \div 512$
A_3	$f_0 \div 8$	$\overline{CS}$	$f0 \div 1024$ (pulse mode)
A_4	$f_0 \div 16$		
A_5	$f_0 \div 32$	or $\overline{CS}$(PE)= V_{IH} (de-select mode)	
A_6	$f_0 \div 64$		

3. Device under test may be operated with $\overline{CS}$(PE) input pulsed or at V_{IH}.

FIGURE 5. Burn-in and operation life test circuit.



NOTES:
1. The $\overline{CS}$(PE) transition must occur after the program pulse transition and before the address transition.
2. See 4.7 herein for programming procedure.

FIGURE 6. Programming waveforms.

TABLE III. Group A inspection.

Subgroup	Symbol	MIL-STD-883 method	Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Meas. terminal	Test Limits		
				A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Q_1	Q_2	Q_3	V_{SS}	Q_4	Q_5	Q_6	Q_7	Q_8	P	V_{DD}	$\overline{CS}$(PE)	V_{BB}	A_9	A_8	V_{CC}		Min	Max	Unit
1 T_C = 25°C	V_{OH1}	3006	1	1/	1/	1/	1/	1/	1/	1/	1/	-100 µA	-100 µA	-100 µA	GND	-100 µA	-100 µA	-100 µA	-100 µA	-100 µA	GND	10.8 V	GND	-4.5 V	1/	1/	4.5 V	Q_1	3.7		V
			2																									Q_2			
			3																									Q_3			
			4																									Q_4			
			5																									Q_5			
			6																									Q_6			
			7																									Q_7			
			8																									Q_8			
	V_{OH2}		9									-1.0 mA	-1.0 mA	-1.0 mA		-1.0 mA	-1.0 mA	-1.0 mA	-1.0 mA	-1.0 mA								Q_1	2.4		
			10																									Q_2			
			11																									Q_3			
			12																									Q_4			
			13																									Q_5			
			14																									Q_6			
			15																									Q_7			
			16																									Q_8			
	V_{OL}	3007	17									1.6 mA	1.6 mA	1.6 mA		1.6 mA	1.6 mA	1.6 mA	1.6 mA	1.6 mA		13.2 V		-5.5 V			5.5 V	Q_1		0.45	
			18																									Q_2			
			19																									Q_3			
			20																									Q_4			
			21																									Q_5			
			22																									Q_6			
			23																									Q_7			
			24																									Q_8			
	I_{LO} 2/		25									5.5 V	5.5 V	5.5 V		5.5 V							2.4 V					Q_1		10	µA
			26																									Q_2			
			27																									Q_3			
			28																									Q_4			

See footnotes at end of table.

TABLE III. Group A inspection - Continued.

Subgroup	Symbol	MIL-STD-883 method	Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Meas. terminal	Test limits		
				A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_1	O_2	O_3	V_{SS}	O_4	O_5	O_6	O_7	O_8	P	V_{DD}	$\overline{CS}$(PE)	V_{BB}	A_9	A_8	V_{CC}		Min	Max	Unit
$T_C = 25°C$	I_{LO} 2/		29	V	V	V	V	V	V	V	V				GND		5.5 V	5.5 V	5.5 V	5.5 V	GND	13.2 V	2.4 V	-5.5 V	V	V	5.5 V	O_5		10	µA
			30																									O_6			
			31																									O_7			
			32																									O_8			
	I_{IH}	3010	33	5.5 V																								A_7			
			34		5.5 V																							A_6			
			35			5.5 V																						A_5			
			36				5.5 V																					A_4			
			37					5.5 V																				A_3			
			38						5.5 V																			A_2			
			39							5.5 V																		A_1			
			40								5.5 V																	A_0			
			41																									$\overline{CS}$(PE)			
			42																				5.5 V					A_9			
			43																						5.5 V			A_8			
	I_{IL}		44	0.05 V																								A_7			
			45		0.05 V																							A_6			
			46			0.05 V																						A_5			
			47				0.05 V																					A_4			
			48					0.05 V																				A_3			
			49						0.05 V																			A_2			
			50							0.05 V																		A_1			
			51								0.05 V																	A_0			
			52																									$\overline{CS}$(PE)			
			53																				0.05 V					A_9			
			54																						0.05 V			A_8			
	I_{OS} 3/	3011	55	V	V	V	V	V	V	V	V	GND			GND								0.05 V	V	V	V		O_1	-30		
		3011	56	V	V	V	V	V	V	V	V		GND		GND								0.05 V	V	V	V		O_2	-30		

See footnotes at end of table.

TABLE III. Group A inspection - Continued.

Subgroup	Symbol	MIL-STD-883 method	Test No.	1 A_7	2 A_6	3 A_5	4 A_4	5 A_3	6 A_2	7 A_1	8 A_0	9 Q_1	10 Q_2	11 Q_3	12 V_{SS}	13 Q_4	14 Q_5	15 Q_6	16 Q_7	17 Q_8	18 P	19 V_{DD}	20 $\overline{CS}$(PE)	21 V_{BB}	22 A_9	23 A_8	24 V_{CC}	Meas. terminal	Test Limits Min	Max	Unit
1 T_C = 25°C	I_{DS} 3/	3881	57	3/	3/	3/	3/	3/	3/	3/	3/			GND		GND	GND				13.2 V	6.65 V	-6.5 V	3/	3/	5.5 V	Q_3		-30	mA
			58																								Q_4			
			59																								Q_5			
			60																								Q_6			
			61																								Q_7			
			62																								Q_8			
	I_{BB}	3805	63	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	3/	3/	3/		3/	3/	3/	3/	3/	GND			2.4 V	2.4 V		V_{BB}		50	
	I_{CC}	3805	64	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	3/	3/	3/		3/	3/	3/	3/	3/	GND			2.4 V	2.4 V		V_{CC}		15	
	I_{BB}	3805	65	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V	3/	3/	3/		3/	3/	3/	3/	3/	GND			2.4 V	2.4 V		V_{BB}		80	
2	Same tests, terminal conditions and limits as for subgroup 1, except T_C = +100°C.																													
3	Same tests, terminal conditions and limits as for subgroup 1, except T_C = -55°C.																													
7 T_C = 25°C	Functional tests	3014	66	3/	3/	3/	3/	3/	3/	3/	3/	3/	3/	3/	3/	3/	3/	3/	3/	3/	3/	3/	3/	3/	3/	3/	3/	All outputs			
8	Same tests, terminal conditions and limits for subgroup 7, except T_C = +100°C and -55°C.																													
9 T_C = 25°C	t_{PZH}		67	3/	3/	3/	3/	3/	3/	3/	3/	3/	3/	3/	3/	3/	GND	3/	3/	3/	3/	3/	GND	11/		11/	11/	11/	11/	Outputs		11/	ns
	t_{PHZ}		68																												
	t_{PZL}		69																												
	t_{PLZ}		70																												
	t_{PLH}		71																												
	t_{PHL}		72																												
10	Same tests, terminal conditions and limits as for subgroup 9, except T_C = +100°C.																													
11	Same tests, terminal conditions and limits as for subgroup 9, except T_C = -55°C.																													

1/ Before performing electrical tests, a binary count pattern shall be programmed into the devices submitted for acceptance. V_{IH} (2.4 V) or V_{IL} (0.65 V) shall be applied to the applicable address pins to set the measured terminal in the proper state for measurement.

2/ Connect all address inputs and the $\overline{CS}$(PE) input to V_{IH} and measure I_{LI} with the output under test connected to the voltages specified.

3/ Connect the $\overline{CS}$(PE) input to V_{IL}. Condition the address inputs to set the output under test indicated "H" per the checkerboard truth table* to its high voltage state and measure I_{DS} with the output under test connected to ground.

4/ Output pins (Q1 thru Q8) shall be open.

5/ Inputs shall verify binary count pattern. All bits shall be tested with the following conditions:
   a. V_{CC} = 5.5 V, V_{BB} = -6.5 V, V_{DD} = 13.2 V
   b. V_{CC} = 4.5 V, V_{BB} = -4.5 V, V_{DD} = 10.8
   c. Inputs: H = 2.4 V, L = GND
   d. Outputs: Output voltage shall be either:
      1. H = 2.4 V minimum and L = 0.5 V maximum when using a high speed checker double comparator.
      2. H ≥ 1.0 V and L ≤ 1.0 V when using a high speed checker single comparator.

6/ Each output shall be connected to the load circuit shown on figure 4 and propagation delay times shall be measured as follows:
   a. Address inputs to outputs. Set the $\overline{CS}$(PE) input to ground. Measure t_{PLH} and t_{PHL} from each address input to each output. Output under test shall be alternately changed from its low level to its high level by addressing the appropriate word combinations.
   b. $\overline{CS}$(PE) input to programmed outputs. Condition address inputs A_0 thru A_9 to set outputs under test to the "L" state. Pulse $\overline{CS}$(PE) input and measure t_{PLZ} and t_{PZL}.
   c. $\overline{CS}$(PE) input to unprogrammed outputs. Condition address inputs A_0 thru A_9 to set outputs under test to the "H" state. Pulse $\overline{CS}$(PE) input and measure t_{PHZ} and t_{PZH}.

11/ See table I herein for supply voltages and test limits.

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4.4.3 Group C inspection. Group C inspection shall be in accordance with table II of method 5005 of MIL-STD-883 and as follows:

a. End point electrical parameters shall be as specified in table II.

b. Steady state life test (method 1005 of MIL-STD-883) conditions:

1. Test condition D or E using the circuit shown on figure 5, or equivalent.

2. T_A = +100°C, minimum.

3. Test duration: 1000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

4. All devices selected for testing shall be programmed with a binary count pattern. After completion of all testing, the devices shall be erased and verified (except devices submitted for group D testing).

c. A reprogrammability test shall be added to group C inspection prior to performing the steady state life test (see 4.4.3b). The devices to be submitted to the steady state life testing shall be subjected to the following tests and examinations:

1. Each device in the sample shall be subjected to a minimum of 50 program and erase cycles. Each cycle shall consist of the following steps:

a. Program all devices with a binary count pattern.

b. Verify pattern (see 3.7.3).

c. Erase (see 3.7.1).

d. Verify pattern (see 3.7.3).

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883 and as follows:

a. End point electrical parameters shall be as specified in table II.

b. All devices selected for testing shall be programmed with a binary count pattern. After completion of all testing the devices shall be erased and verified.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Packing inspection. The sampling and inspection of the preservation-packaging, packing and container marking shall be in accordance with the requirements of MIL-M-38510, except that the rough-handling test shall not apply.

4.7 Programming procedure. The following procedures shall be followed when programming and verification testing is performed. The waveforms and timing relationships shown in figure 6 and the test conditions and limits specified in table IV shall be adhered to.

a. Initially, and after each erasure, all bits are in the "H" state (output high). Information is introduced by selectively programming "L" into the desired bit locations. A programmed "L" can only be changed to an "H" by ultraviolet light erasure.

b. The circuit is set up for programming operation by raising the $\overline{CS}$(PE) input (pin 20) to +12 V. The word address is selected in the same manner as in the read mode. Data to be programmed, 8-bits in parallel, are presented to the data lines (Q_1-Q_8). Logic levels for address and data lines, and the supply voltages are the same as for the read mode. After address and data set up, one program pulse per address is applied to the program input (pin 18). One pass through all addresses is defined as a program loop. The number of loops (N) required is a function of the program pulse width (tpW) according to N x tpW $\geq$ 100 ms.

c. The width of the program pulse is from 0.1 to 1 ms. The number of loops (N) is from a minimum of 100 (tpW = 1 ms) to greater than 1,000 (tpW = 0.1 ms). There must be N successive loops through all 1,024 addresses. It is not permitted to apply N program pulses to an address and then change to the next address to be programmed. Caution should be observed regarding the end of a program sequence. The $\overline{CS}$(PE) falling edge transition must occur before the first address transition when changing from a program to a read cycle. The program pin should also be pulled down to V_{ILP} with an active instead of a passive device. This pin will source a small amount of current (I_{ILP}) when $\overline{CS}$(PE) is at V_{IHW} (12 V) and the program pulse is at V_{ILP}.

d. Programming examples (using N x tpW $\geq$ 100 ms):

Example 1: All 8,192 bits are to be programmed with a 0.5 ms program pulse width. The minimum number of program loops is 200. One program loop consists of words 0 to 1,023.

Example 2: Words 0 to 100 and 500 to 600 are to be programmed. All other bits are "don't care". The program pulse width is 0.75 ms. The minimum number of program loops is 133. One program loop consists of words 0 to 1,023. The data entered into the "don't care" bits should be all H's.

Example 3: Same requirements as example 2 but the PROM is now to be updated to include data for words 750 to 770. The minimum number of program loops is 133. One program loop consists of words 0 to 1,023. The data entered into the "don't care" bits should be all H's. Addresses 0 to 100 and 500 to 600 must be reprogrammed with their original data pattern.

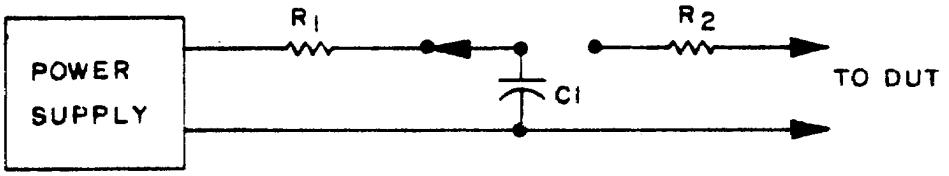
4.8 Erasing procedure. The device is erased by exposure to high intensity short wave ultraviolet light at a wavelength of 253.7 nm. The recommended integrated dose (i.e., UV intensity x exposure time) is 15 W-s/cm^2. An example of an ultraviolet source which can erase the device in 30 minutes is the model S52 short wave ultraviolet lamp. The lamp should be used without short wave filters and the EPROM should be placed about 1 inch away from the lamp tubes. After erasure all bits are in the high state.

4.9 High voltage (V_{ZAP}) test of input protection circuits. One input terminal of the device under test (DUT) shall be subjected to a voltage pulse of 150 volts from a 100-picofarad source in the following test sequence:

a. Measure I_{IH} and I_{IL} at one input terminal of the DUT at 25°C. Also measure I_{BB} at 25°C. These measurements shall be made in accordance with table III herein. The test limits for a single terminal measurement of I_{IH} and I_{IL} shall be ±10 µA, maximum.

b. In the circuit below, charge the capacitor to -150 V. Then, using the same terminal of the device as selected above for leakage measurements, switch the capacitor to discharge into the device terminal. Then repeat the procedure with +150 V. (See figure 7).

c. Within 24 hours, repeat the I_{BB} measurement and I_{IH} and I_{IL} measurements on the same terminal as performed above. At this time a DUT exhibiting leakage currents in excess of the specified limits is defective.



R_1 = Appropriate current-limiting resistance
R_2 = 1.5 kΩ ±5%.
C1 = 100 pF ±20%.
Power supply voltage = V_{zap} = +150 Vdc and -150 Vdc.

FIGURE 7. High voltage (V_{ZAP}) test.

TABLE IV. Programming characteristics.

Parameter	Symbol	Conditions V_{CC} = 5.0 V, V_{BB} = -5.0 V, V_{DD} = 12 V, V_{SS} = 0 V, V_{IH} = 3.0 V min, V_{IL} = 0.65 max, V_{IHW} ($\overline{CS}$(PE)) = 12 V ±5%, T_C = +25°C	Limits		Units
			Min	Max	
Program pulse high current	I_{IHP}	V_{IHP} = 26 ±1 V		40	mA
Program pulse low current	I_{ILP}	V_{ILP} = 0 V, V_{IHP} - V_{ILP} = 25 V min		3	mA
Address setup time	t_{AS}	See figure 6 and 4.7	10		µs
$\overline{CS}$(PE) setup time	t_{CSS}		10		µs
Data setup time	t_{DS}		10		µs
Address hold time	t_{AH} 1/		1		µs
$\overline{CS}$(PE) hold time	t_{CH}		0.5		µs
Data hold time	t_{DH}		1		µs

See footnote at end of table.

TABLE IV. Programming characteristics - Continued.

Parameter	Symbol	Conditions	Limits		Units
			Min	Max	
		V_{CC} = 5.0 V, V_{BB} = -5.0 V, V_{DD} = 12 V, V_{SS} = 0 V, V_{IH} = 3.0 V min, V_{IL} = 0.65 max, V_{IHW} ($\overline{CS}$(PE)) = 12 V ±5%, T_C = +25°C			
Chip deselect to output float delay	t_{DF}	See 4.7	0	120	ns
Program to read delay	t_{DPR}	See figure 6 and 4.7		10	µs
Program pulse width	t_{PW}		0.1	1.0	ms
Program pulse rise time	t_{PR}		0.5	2.0	µs
Program pulse fall time	t_{PF}		0.5	2.0	µs

1/ Minimum time from data input stop to address 1023 change is 0 ns.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510. The devices covered by this specification require electrostatic protection.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use for Government microcircuit applications (original equipment) and logistic purposes.

6.3 Ordering data. The contract should specify the following:

a. Complete part number (see 1.2).

b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

c. Requirement for certificate of compliance, if applicable.

d. Requirements for notification of change of product or process to procuring activity in addition to notification to the qualifying activity, if applicable.

e. Requirements for packaging and packing.

f. Requirements for failure analysis (including required test condition of MIL-STD-883, method 5003), corrective action and reporting of results, if applicable.

g. Requirements for product assurance options.

h. Requirements for carriers, special lead lengths or lead forming, if applicable. These requirements shall not affect the part number, unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.

6.4 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-STD-1313, MIL-STD-1331, and as follows:

$t_{c(rd)}$	Read cycle time
t_{pvx}	Output invalid address change
V_{IN}	Voltage level at an input terminal
I_{IN}	Current flowing into an input terminal

6.5 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits procured for Government logistic support will be procured to device class B (see 1.2.2), and lead material and finish C (see 3.3). Longer length and lead forming shall not affect the part number.

6.6 Handling. MOS devices must be handled with certain precautions to avoid damage due to accumulation to static charge. Input protective devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

a. Devices should be handled on benches with conductive and grounded surface.

b. Ground test equipment and tools.

c. Do not handle devices by the leads.

d. Store devices in conductive foam or carriers.

e. Avoid use of plastic, rubber, or silk in MOS area.

f. Maintain relative humidity above 50 percent, if practical.

6.7 Generic test data. Generic test data may be used to satisfy the requirements of 4.4.3. Group C generic test data shall be on date codes no more than one year old and on a die in the same microcircuit group (see appendix E of MIL-M-38510) with the same material, design and process from the same plant as the die represented. Group D (see 4.4.4) generic data shall be on date codes no more than one year old and on the same package type (see terms, definitions, and symbols of MIL-M-38510) and from the same plant as the packaged represented. The vendor is required to retain generic data for a period of not less than 36 months from the date of shipment.

6.8 Ordering guidance. Since the qualification and certification requirements have been removed from the specification, orders may be placed immediately.

6.9 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

6.10 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military device type	Generic-industry type
01	2708

Custodian:
Air Force - 17

Review activities:
Air Force - 11, 19, 85, 99
DLA - ES

Agent:
DLA - ES

Preparing activity:
Air Force - 17

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